Amendments to the Specification:

Please amend the paragraph beginning on page 6, line 24 with the following amended paragraph:

With reference in particular to Figure 1, an Analog-To-Digital (ADC) converter 100 is shown. The converter 100 receives a (~~continuos~~ continuous) wide-band analog input signal, denoted with X(z) in the z-transform domain; the analog input signal X(z) is oversampled at a relatively low OSR, such as 4 or 8. The analog input signal X(z) is converted into a corresponding digital output signal U(z), which consists of discrete samples taken at evenly spaced intervals.

Please amend the paragraph beginning on page 12, line 5 with the following amended paragraph:

Moving now to Figure 3, the logic module 210 includes a digital (or ~~sinc~~ sync) filter 310 receiving the digital output signal $Y_0(z)$ from the pipeline stage. The ~~sinc~~ sync filter 310 calculates the mean value of a number of samples of the digital output signal $Y_0(z)$, as defined by a decimation parameter (for example, 128). The result of this operation consists of a digital signal that is proportional to a residual error caused by the offset (of the flash ADC in the sigma-delta converter) still to be corrected; the digital residual error has a high resolution equal to the one of the whole pipeline stage (i.e., 9 bits). A quantizer 320 discards the least significant bits of the digital residual error, so as to reduce its resolution to the desired value (5 bits in the example at issue).

Please amend the paragraph beginning on page 13, line 1 with the following amended paragraph:

The decimation parameter of the ~~sinc~~ sync filter 310 defines the precision and the convergence speed of the process. High values of the decimation parameter increase the number of samples taken into consideration at every estimation step, and then also the precision of the ~~sinc~~ sync filter 310; however, this slows down the convergence speed of the process (since the digital correction signal crt is updated with a lower frequency). Conversely, low values of the decimation parameter increase the convergence speed of the process, but reduce its precision.

Please amend the paragraph beginning on page 14, line 1 with the following amended paragraph:

In order to perform the above-mentioned comparisons, the flash ADC 115 includes an even number of comparators 410 (only one explicitly shown in the figure but a plurality of comparators being indicated by the ellipses 411), which comparators operate in parallel. Each comparator 410 is actuated by a latching signal Φ_l. The comparator 410 has a non-inverting input terminal (+), which is connected to a ground terminal through an electronic switch 420i (for example, implemented with a MOS transistor); the switch 420i is controlled by a pre-charging signal Φ_p. Likewise, an inverting input terminal (-) of the comparator 410 is connected to the ground terminal through a switch 420t, which is controlled by the same pre-charging signal Φ_p.